REMARKS/ARGUMENTS

In the Office Action, the Examiner has rejected claims 1-8 and 10-16 under 35 U.S.C. §103(a) as being unpatentable over Wang in view of U.S. Patent 6, 385,267 (hereinafter referred to as Bowen).

The Applicant respectfully submits that the subject matter claimed in claims 1-7 and 10-16, as amended, distinguishes patentably over the cited prior art references, as discussed below.

We have amended claim 1. This amendment is made for clarification purposes only, as it is not needed for patentability, and does not change the scope of the claim.

Support for the amendment can be found throughout, and specifically as set out below.

For ease of reference, claim 1, showing the amendments, is set out below.

11. A synchronizer for mapping an electrical digital signal of **arbitrary transmission rate for transport over a network** characterized by a ~~range~~ set of allowable transmission rates, ***said arbitrary transmission rate not being restricted to said set of allowable transmission rates,*** said synchronizer comprising:

a) an input for receiving the electrical digital signal;

b) a data recovery unit coupled to said input, said data recovery unit operative to recover from the electrical digital signal a stream of data bits and a first data clock signal indicative of the arbitrary transmission rate;

c) a clock generator unit coupled to said data recovery unit, said clock generator including a first input for receiving the first data clock signal and a second input for receiving a control signal, said clock generator unit being operative to multiply a frequency of the first data clock signal by a value indicated by the control signal for generating a second data clock signal, ~~whereby~~ the second data clock signal ~~is~~ *being* indicative of a line transmission rate that falls within the ~~range~~ set of allowable transmission rates for the network;

d) a mapping unit in communication with said clock generator unit for receiving the second data clock signal, said mapping unit being operative for mapping the stream of data bits into at least one frame at a line transmission rate indicated by the second data clock signal; and

e) an output for releasing the at least one frame from said synchronizer for transmission over the network.

As quoted in our response of June 7, 2005, quoting from the background section of the present application:

> the **line rates** for these networks have been **restricted to a set of discrete transmission rates**. Similarly, current electrical transport networks, such as the DS3 electrical network, are also limited to particular, discrete transmission rates. Thus, **data characterized by a transmission rate that does not belong to the set of pre-defined transmission rates is not directly transportable over such data networks.** In many cases, a user signal must undergo a mapping operation to be able to be transported by the data network.

Claim 1 has been amended to change "***range*** of allowable transmission rates" to "set of allowable transmission rates" to have language consistent with this passage. However, this is not needed for patentability reasons, as it is submitted that no change of scope is made or intended.

Quoting from pg 5 lines 19 -24 of the present application:

> "Thus, an electrical digital signal of arbitrary transmission rate, where this arbitrary transmission rate does not fall within the range of allowable transmission rates for the data network, may be transparently transported over the data network."

This clearly demonstrates that the arbitrary transmission rate is not restricted to the set of allowable transmission rates for the network. It is submitted that this is what is meant by arbitrary transmission rate. The amendment merely clarifies the language of the claim. This amendment is not necessary for patentability, as it is submitted that is there is no change of scope, as this is the proper interpretation of the claim.

In traversing the rejection to the claims, we reiterate our arguments, namely:

1) No Prima Facie Case of obviousness;

2) Wang does not disclose, teach or even suggest a system capable of mapping or synchronizing input signals of arbitrary rates; and

3) Even if it is proper to combine the Wang and Bowen references, such a combination will not work, as Wang is not directed to arbitrary rates, but to a set of discrete rates, and will not work for an arbitrary rate.

The Applicant respectfully submits that Wang and Bowen, whether taken alone or in combination, do not disclose, teach nor suggest the invention claimed in claim 1. Without limiting the generality of the foregoing, neither reference teaches a system for mapping a signal having an **arbitrary transmission rate.**

As stated in the background section of the present application, the mapping of one rate or format into another is well known. However, the prior art systems are restricted to mapping signals of very specific rates, typically based on Plesiochronous Digital Hierarchy (PDH), as discussed in the background section of the present application:

> "Originally, optical transport networks were intended to be bit-rate and data format independent, thus providing for the transportation of a wide variety of data signals. Unfortunately, current optical transport networks, including SONET/SDH networks, do not achieve this goal, as the **line rates** for these networks have been **restricted to a set of discrete transmission rates**. Similarly, current electrical transport networks, such as the DS3 electrical network, are also limited to particular, discrete transmission rates. Thus, **data characterized by a transmission rate that does not belong to the set of pre-defined transmission rates is not directly transportable over such data networks.** In many cases, a user signal must undergo a mapping operation to be able to be transported by the data network.
>
> The mapping of one rate or format into another is well known. For example, Bellcore TR-0253 describes in detail the standard mappings of the common
>
> asynchronous transmission formats (DS0, DS1, DS2 and DS3, among others) into SONET. Similar mappings are defined for the ETSI hierarchy mapping into SDH.

Unfortunately, **the standards or proprietary schemes allow the transportation of only a very specific set of signals, with format specific hardware.** Thus, these methods of mapping **cannot** be used to **map rates that vary significantly from the standard.** Furthermore, these **mappings** are each **precisely tuned for a particular format and a particular bit-rate,** with for example a ±20ppm (parts per million of the bit rate) tolerance. If a signal has, for example, a bit rate even 1% different than that of a DS3, it cannot be transported over a SONET/SDH network. In addition, a different hardware unit is generally required to perform the mapping of each kind of signal." (emphasis added) (col 2, l 15-Column 3- line 13).

Neither reference discusses this problem or any solution to it.

Wang relates to multiplexing one or several lower rate signals into a higher rate signal in digital communication systems. The multiplexing of the lower rate signals can introduce a form of phase variation or jitter into the signals referred to as waiting time jitter. Wang relates to removing waiting time jitter from the signals. (Field of the Invention). It does address multiplexing plural lower rate signals into a higher rate signal, but it does this for conventional signals (i.e. for a set of discrete transmission rates). See background section generally, and in particular Column 2 lines 5-15, and Column 3, lines 8-10 wherein Wang describes the problem to be solved with reference to an example of a DS1 to DS2 mapping.

In the examiner's response to applicant's arguments, the examiner quotes from the abstract of Wang, which discloses that the input data signal is a "lower rate signal that is plesiochronous with a higher rate signal into which the lower rate signal is to be multiplexed".

However, that does not rebut our arguments – that is the point of our arguments. Wang only teaches a system of synchronizing Plesiochronous signals, according to specific to specific rate mappings, as discussed.

Then the examiner equates the lower rate discussed in Wang as an arbitrary rate. It is not, and this will be shown below. However, by doing this the examiner completely ignored the invention, and the problem which it solves, which is the ability to map signals regardless of whether the incoming signal is **restricted to the set of allowable transmission rates.**

As stated above, the claim language has been clarified to indicate that the arbitrary *rate is **not restricted to said set of allowable transmission rates**. **Once again, we reiterate this does not change the scope of the claim, as this was what arbitrary transmission rate meant in the rejected claim.***

Wang is simply not capable of dealing with incoming signals of arbitrary rates. It is clearly restricted to handling signals of fixed formats, with defined bit stuffing positions. This is clear throughout Wang, and is evidenced in the following sample passages:

> "The data bits read out in synchronism with the gapped read clock are placed in the payload bit positions of the corresponding channel" (Col. 4, line 32-34).
>
> "The range may be adjusted to produce optimum threshold values for a given synchronizer (i.e. knowing ahead of time the data rates of the lower and higher rate signals, the organizations of the lower and higher rate signals into payload data bits, stuffing bits and overhead control bits, and the permissible phase tolerances for each of these signals)."
> (Col 7, lines 13-19)
>
> "To facilitate dividing the bits into time slots, a frame timing signal is inputted to the logic gate 145 for enabling the reading out of bits from the elastic buffer 120 only during payload and stuffing bit positions of the time slots corresponding to the lower rate signal" (col.10, lines 11-15).
>
> "In addition, a frame timing signal is outputted which has pulses corresponding to the payload and data-bit carrying stuffing bit position of the higher rate signal and gaps corresponding to control bit positions and null-stuffing bit positions of the higher rate signal. (col 10, lines 34-38)

Accordingly, Wang does not teach the claimed invention in the way characterized by the rejection. The rejection appears to state that Wang teaches every element except for disclosing a clock generator performing frequency multiplication of the first clock on a first

input and a control signal on a second input for generating a second clock. However, Wang also fails to teach at least elements b, c, and d of claim 1.

In any event, we reiterate our arguments that the rejection fails to establish a prima-facie case.

In the examiner's response, it is stated that Bowen is only used to show that frequency multiplication is known, and that it would be obvious for a person skilled in the art to combine the references to achieve the claimed invention.

The passages in Bowen relate to phase locked loops. These passages teach the use of frequency multiplication in order to phase lock signals – and is simply not relevant to the claimed invention, or even the teachings of Wang.

In our response of June 7, 2005, we argued that the rejection was improper, as it failed establish a prima facie case, as it failed to it to demonstrate any suggestion to combine, or any evidence for a motivation to combine the references. We reiterate this argument.

In addition, even if it was proper to combine these references (which is denied), such a combination fails to teach the claimed invention. In any event, such a combination would simply not work for an arbitrary rate, but would be limited to fixed rate signals, for the same reasons that Wang is not capable of synchronizing signals or arbitrary rates.

This is true for the original claimed language. In any event, the references certainly do not teach, or suggest the invention of the amended claims.

Accordingly, withdrawal of the rejection and allowance of the application is solicited.

The Commissioner is hereby authorized to charge any additional fees, and credit any over payments to Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP.

Respectfully submitted,

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